(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 372 526 A2**

# (12) EUROPEAN PATENT APPLICATION

(21) Application number: 89122485.9

(51) Int. Cl.5: H03M 1/12, G06F 3/05

(22) Date of filing: 06.12.89

(30) Priority: 06.12.88 JP 309292/88

(43) Date of publication of application: 13.06.90 Bulletin 90/24

(84) Designated Contracting States: DE FR GB

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## (54) Microcomputer having high speed a/d conversion function.

(57) A microcomputer includes an central processing unit and an A/D conversion circuit formed on the same integrated circuit chip. The microcomputer comprises a plurality of sample and hold circuits coupled to receive, sample and hold an analog voltage, and a timer coupled to the plurality of sample and hold circuits for supplying a analog voltage sampling timing signal to the sample and hold circuits. The sample and hold circuits is coupled through a gate circuit to the A/D conversion circuit so that the analog voltages held in the sample and hold circuits is sequentially selected one by one, and the selected one is supplied to the A/D conversion circuit so that the A/D conversion circuit sequentially converts the analog voltages held in the sample and hold circuits into a digital data one by one.

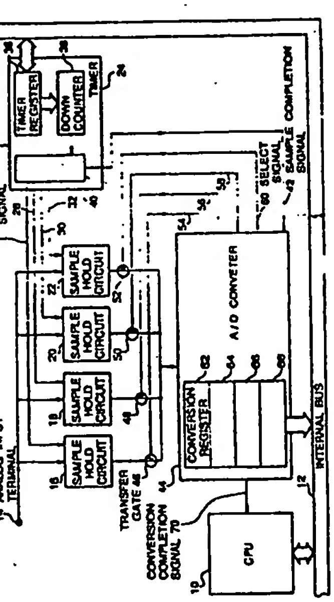


FIGURE 1

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# MICROCOMPUTER HAVING HIGH SPEED A/D CONVERSION FUNCTION

## Background of the Invention

### Field of the invention

The present invention relates to a microcomputer, and more specifically to a microcomputer containing an analog-to-digital (A/D) conversion function therein.

### Description of related art

Conventionally, a head for data reading and writing of hard disks and floppy disks has been positionally servo-controlled to trace a track on the disk. This servo-control has been effected by obtaining a current head position by detecting a servo-pattern previously recorded between a data region and an adjacent data region on the track, in synchronism with and with reference to a termination of each data region, and by deriving a difference between the detected head position and a target track so as to modify the position of the head.

Here, assume that four data tracks A, B, C and D are concentrically formed at different radii on a disk, and the data tracks A, B, C and D respectively include data regions A1, B1, C1 and D1 which are located in the same sector zone and are angularly separated from data regions A2, B2, C2 and D2 in an adjacent sector zone, with servo patterns PA, PB, PC and PD being interposed between the data regions A1, B1, C1 and D1 and the data regions A2, B2, C2 and D2, respectively. Therefore, these servo patterns PA, PB, PC and PD are detected by a head in the course of movement of the head from an end of the data regions A1, B1, C1 and D1 to a beginning of the data regions A2, B2, C2 and D2.

However, these servo patterns PA, PB, PC and PD are located at different angular positions within an angular zone between the sector zone including the data regions A1, B1, C1 and D1 and the sector zone including the data regions A2, B2, C2 and D2. Therefore, the servo pattern PA is detected at a timing TA after the end of the data region A1 is detected, and after the end of the data region B1 is detected, the servo pattern PB is detected at a timing TB different from the timing TA. In addition, after the end of the data region C1 is detected, the servo pattern PC is detected at a timing TC different from each of the timings TA and TB, and after the end of the data region D1 is detected, the servo pattern PD is detected at a timing TD different from each of the timings TA, TB and TC. Therefore, the position of the head can be detected by converting into a digital signal an analog read signal outputted from the head when the head passes in front of a position corresponding to the timing TA, TB, TC or TD after the head has passed the end of the sector zone including the data regions A1, B1, C1 and D1.

For example, here assuming that the head is on the track C, after the head detects the end of the sector zone including the data regions A1, B1, C1 and D1, reading signals outputted from the head at the timings TA, TB and TD are almost 0V, respectively, and on the other hand, a reading signal outputted from the head at the timing TC becomes about 5V. As a result, it is detected that the head is on the track C. In addition, even if the head is at an intermediate position between tracks, the position of the head can be determined by examining the reading signal outputted from the head.

However, it has been an ordinary practice that an area for the servo pattern is in a range corresponding to several hundred microseconds, and a width of the servo pattern itself substantially corresponds to 100 microseconds. Therefore, even in the case that the head position discrimination on the basis of digital information obtained by an analog-to-digital (A/D) conversion of the reading signal outputted from the head is allowed to be considerably delayed in time, since the change of the analog voltage occurs in a very short time, a high speed A/D converter such as a flash type A/D converter has been required. Accordingly, it has not been possible to use a relatively inexpensive successive approximation A/D converter.

The flash type A/D converter can execute an A/D conversion at one time, but needs $2^8$ comparators for A/D conversion in a 8-bit resolution, for example. Therefore, the flash type A/D converter is very expensive and requires a large chip size. Accordingly, it has not been possible to assemble the flash type A/D converter on a single chip microcomputer. In other words, application systems have been expensive.

In addition, since it has been necessary to provide a discrete A/D converter independently of a microcomputer, the microcomputer has to be coupled to receive an output of the A/D converter for the purpose of discriminating the position of the head. As a result, the board size has been inevitably large, and an increased cost for wiring has been required. Further, reliability has been low.

In the prior art, furthermore, when a plurality of analog inputs must be converted into a digital

signal at the same timing, respectively, it has been required to provide a corresponding number of A/D converters. Therefore, a further increased cost has been required.

As mentioned above, in the conventional A/D converter systems, an expensive A/D converter for conversion of an input analog signal varying in a short time has to have been provided externally of a microcomputer. As a result, application systems have required an increased cost for integrated circuits, and therefore, have not been so economical and could not have a satisfactory reliability.

## Summary of the Invention

Accordingly, it is an object of the present invention to provide a microcomputer having an A/D conversion function, which has overcome the above mentioned defect of the conventional one.

Another object of the present invention is to provide a microcomputer having an A/D conversion function, which is inexpensive and can convert into a digital signal an analog signal which varies in a short time.

The above and other objects of the present invention are achieved in accordance with the present invention by a microcomputer which includes an central processing unit and an A/D conversion circuit formed on the same integrated circuit chip, comprising a plurality of sample and hold circuits coupled to input means for sampling and holding an analog voltage supplied through the input means, timing generation means coupled to the plurality of sample and hold circuits for supplying a analog voltage sampling timing signal to the sample and hold circuits, means coupled to the timing generation means for initializing the timing generation means, and means coupled to the sample and hold circuits and the A/D conversion circuit for sequentially selecting one of the analog voltages held in the sample and hold circuits and supplying the selected one to the A/D conversion circuit, so that the A/D conversion circuit sequentially converts the analog voltages held in the sample and hold circuits into a digital data one by one.

According to another aspect of the present invention, there is provided an A/D conversion circuit comprising:

a plurality of sample and hold circuits each having an analog signal input, a sample timing control input and an output, each of the sample and hold circuits responding to a sample timing signal applied to the sample timing control input, so as to sample and hold an analog voltage applied to the analog signal input, so that the analog voltage held in the sample and hold circuit is outputted from the output of the sample and hold circuit;

an A/D converter provided commonly to the plurality of sample and hold circuits and having an input for selectively sequentially receiving the outputs of the sample and hold circuits one by one, so as to sequentially convert the received analog voltage into a digital data; and

timing control means for supplying the sample timing signal to the sample timing control input of the sample and hold circuits, so that the sample and hold circuits sample and hold the analog voltages applied to the analog signal inputs of the sample and hold circuits, the timing control means supplying a sample completion signal to the A/D converter after all the sample and hold circuits have sampled and held the analog voltages applied to the analog signal inputs of the sample and hold circuits, so that the A/D converter starts its A/D conversion after all the sample and hold circuits have sampled and held the analog voltages applied to the analog signal inputs of the sample and hold circuits.

The above and other objects, features and advantages of the present invention will be apparent from the following description of preferred embodiments of the invention with reference to the accompanying drawings:

## Brief Description of the Drawings

Figure 1 is a block diagram of an embodiment of the microcomputer in accordance with the present invention;

Figure 2 is a timing chart illustrating an operation of the microcomputer shown in Figure 1; and

Figure 3 is a block diagram of a modification of the microcomputer shown in Figure 1.

## Description of the Preferred embodiments

Referring to Figure 1, there is shown a block diagram of an embodiment of the microcomputer in accordance with the present invention.

The shown microcomputer includes a central processing unit (CPU) 10 coupled to an internal bus 12, and an analog input terminal 14 commonly coupled to four sample and hold circuits 16, 18, 20 and 22. These four sample and hold circuits 16, 18, 20 and 22 are also coupled to a timer 24 so as to receive sample signals 26, 28, 30 and 32, respectively, so that the four sample and hold circuits 16, 18, 20 and 22 respectively sample and hold a input analog voltage when the sample and hold circuit receives a corresponding sample signal.

The timer 24 is coupled to a trigger terminal 34 so as to be initialized in response to a trigger signal supplied through the trigger terminal 34. The

timer 24 includes a timer register 36 coupled to the internal bus 12 so that the timer register 36 is set with arbitrary data by the central processing unit 10. This timer register 36 is coupled to an down counter 38 so as to output the data set in the timer register 36 to the down counter 38. The down counter 38 is loaded with the data of the timer register 36 in synchronism with the trigger signal 34, and thereafter, operates to count down or decrement the loaded data. When the value of the down counter 38 becomes zero, the down counter 38 generates an output signal to an output control circuit 40, which generates, on the basis of the output from the down counter 38, the above mentioned sample signals 26, 28, 30 and 32 and a sample completion signal 42 indicating that all the sample and hold circuits 16, 18, 20 and 22 have held new analog voltages.

Outputs of the sample and hold circuits 16, 18, 20 and 22 are inputted to an common analog voltage input of an A/D converter 44 through transfer gates 46, 48, 50 and 52, respectively. The A/D converter 44 responds to the sample completion signal 42 to sequentially output select signals 54, 56, 58 and 60 to the transfer gates 46, 48, 50 and 52, respectively, so that the four analog voltages held in the sample and hold circuits 16, 18, 20 and 22 are selectively sequentially supplied to the A/D converter 44 one by one in accordance with the select signals 54, 56, 58 and 60. The selected analog voltage is converted into a digital data by the A/D converter 44, and the digital data is stored in a corresponding one of four conversion registers 62, 64, 66 and 68 provided in the A/D converter 44. When the A/D converter 44 has completed an A/D conversion of all the four analog voltages held in the sample and hold circuits 16, 18, 20 and 22, the A/D converter 44 generates a conversion completion signal 70 to the central processing unit 10. On the other hand, the four conversion registers 62, 64, 66 and 68 are coupled to the internal bus 12 so that contents of the conversion registers 62, 64, 66 and 68 can be read by the central processing unit 10.

Now, operation of the microprocessor will be decribed with reference to Figure 2 showing a timing chart illustrating an operation of the microcomputer shown in Figure 1.

In synchronism with a fall edge of the trigger signal 34, the value previously set in the timer register 36 of the timer 24 is loaded to the down counter 38, and the down counter 38 starts to decrement the loaded value at each predetermined interval, or at each clock. When the value of the down counter 38 becomes "0" or zero, the down counter 38 outputs the signal to the output control circuit 40, which generates the first sample signal 26. The timer 24 repeats the above mentioned decrement operation four times, and sequentially generates the sample signals 26, 28 30 and 32, as shown in Figure 2. An interval T between the fall edge of the trigger signal 34 and a rising edge of the first sample signal 26 are the same as that between rising edges of each pair of adjacent sample signals, and is determined by the set value of the timer register 36 and a decrementing speed or clock of the down counter 38.

Therefore, the output control circuit 40 of the timer 24 respectively generates the sample signals 26, 28 30 and 32 at different timings T, 2T, 3T and 4T after the fall edge of the trigger signal 34. The sample and hold circuit 16, 18, 20 and 22 sample and hold the input analog voltage on the input terminal 14 when the corresponding sample signal is at "1".

The output control circuit 40 of the timer 24 outputs the sample completion signal 42 after generation of all the sample signals 16, 18, 20 and 22. In response to the sample completion signal 42, the A/D converter 44 brings the select signal 54 to "1" so as to open the transfer gate 46, so that the analog value held in the sample and hold circuit 16 is supplied to the A/D converter 44. The result of the A/D conversion of the analog value is stored in the conversion register 62 corresponding to the sample and hold circuit 16. After the result of the A/D conversion is stored in the conversion register, the A/D converter 44 activates a next select signal, namely, brings the select signal 48 to "1".

The above mentioned A/D conversion operation is repeated further three times, so that the result of the A/D conversion of the analog values held in all the sample and hold circuits 16, 18, 20 and 22 are stored in the corresponding conversion registers 62, 64, 66 and 68, respectively. Thereafter, the A/D converter 44 generates the conversion completion signal 70 to the central processing unit 10. In response to the conversion completion signal 70, the central processing unit 10 fetches the contents of the conversion registers through the internal bus 12, and executes a necessary processing on the basis of the result of the A/D conversion.

Since the above mentioned embodiment has only one A/D converter, an analog input varying in a short time can be inexpensively converted into digital data.

Turning to Figure 3, there is shown a modification of the microcomputer shown in Figure 1. Therefore, in Figure 3, elements corresponding or similar to those shown in Figure 1 are given the same Reference Numerals.

As seen from comparison between Figure 1 and 3, the microcomputer shown in Figure 3 is such that the four sample and hold circuits 16, 18, 20 and 22 are coupled to different input terminals 72, 74, 76 and 78, and also coupled to receive a

common sample signal 80 outputted from the timer 24. Therefore, the four sample and hold circuits 16, 18, 20 and 22 simultaneously sample and hold different analog voltages supplied onto the input terminals 72, 74, 76 and 78, respectively. The other construction and operation of the microcomputer shown in Figure 3 are the same as those of the microcomputer shown in Figure 1, and therefore, further explanation will be omitted.

Since the above mentioned second embodiment also has only one A/D converter, a plurality of analog inputs at the same timing can be inexpensively converted into digital data.

In the above mentioned embodiments, the four sample and hold circuits are provided. However, the number of the sample and hold circuits is not limited, and can be freely increased. In addition, the number of analog input terminals can be increased.

Furthermore, the above mentioned embodiments are such that after all the sample and hold circuits have completed the sampling and holding of analog voltages, the A/D conversion is started. However, the above mentioned embodiments can be modified so that the A/D conversion is started as soon as an analog voltage has been held in one of the sample and hold circuits. In addition, in the above mentioned embodiments, the overall operation including the A/D conversion is timed by the trigger signal, but can be synchronized by a signal generated by a timer or other means.

The invention has thus been shown and described with reference to the specific embodiments. However, it should be noted that the present invention is in no way limited to the details of the illustrated structures.

## Claims

1. A microcomputer which includes an central processing unit and an A/D conversion circuit formed on the same integrated circuit chip, comprising a plurality of sample and hold circuits coupled to input means for sampling and holding an analog voltage supplied through the input means, timing generation means coupled to the plurality of sample and hold circuits for supplying a analog voltage sampling timing signal to the sample and hold circuits, means coupled to the timing generation means for initializing the timing generation means, and means coupled to the sample and hold circuits and the A/D conversion circuit for sequentially selecting one of the analog voltages held in the sample and hold circuits and supplying the selected one to the A/D conversion circuit, so that the A/D conversion circuit sequentially converts the analog voltages held in the sample and hold circuits into a digital data one by one.

2. A microcomputer claimed in Claim 1 wherein the plurality of sample and hold circuits are coupled to a common analog input terminal and the timing generation means generates a corresponding number of analog voltage sampling timing signals at different timings of predetermined constant intervals and supplies the corresponding number of analog voltage sampling timing signals to the sample and hold circuits, respectively, so that the sample and hold circuits respectively sample and hold analog voltage on the common analog input terminal at the different timings.

3. A microcomputer claimed in Claim 2 wherein the timing generation means generates the corresponding number of analog voltage sampling timing signals after the timing generation means is initialized by the initializing means, and the timing generation means generates a sample completion signal to the A/D conversion circuit after the timing generation means has completed the generation of the corresponding number of analog voltage sampling timing signals, so that the A/D converter starts its A/D conversion after all the sample and hold circuits have sampled and held the analog voltages applied to the analog signal inputs of the sample and hold circuits.

4. A microcomputer claimed in Claim 1 wherein the plurality of sample and hold circuits are coupled to a corresponding number of analog input terminals and the timing generation means generates a common analog voltage sampling timing signal to the sample and hold circuits, respectively, so that the sample and hold circuits respectively sample and hold analog voltages on the analog input terminals at the same timing.

5. A microcomputer claimed in Claim 1 wherein respective outputs of the sample and hold circuits are coupled to the A/D conversion circuit through a corresponding number of transfer gates, which are controlled by the A/D conversion circuit so as to be sequentially opened so that analog values stored in the sample and hold circuits are sequentially supplied one by one to the A/D conversion circuit.

6. A microcomputer claimed in Claim 1 wherein the A/D conversion circuit includes a plurality of conversion registers corresponding to the plurality of sample and hold circuits, and operates to store an A/D conversion result of the analog value, in the conversion register corresponding to the sample and hold circuit which has supplied the analog value to the A/D conversion circuit.

7. An A/D conversion circuit comprising:
a plurality of sample and hold circuits each having an analog signal input, a sample timing control input and an output, each of the sample and hold circuits responding to a sample timing signal applied to the sample timing control input, so as to

sample and hold an analog voltage applied to the analog signal input, so that the analog voltage held in the sample and hold circuit is outputted from the output of the sample and hold circuit;
an A/D converter provided commonly to the plurality of sample and hold circuits and having an input for selectively sequentially receiving the outputs of the sample and hold circuits one by one, so as to sequentially convert the received analog voltage into a digital data; and
timing control means for supplying the sample timing signal to the sample timing control input of the sample and hold circuits, so that the sample and hold circuits sample and hold the analog voltages applied to the analog signal inputs of the sample and hold circuits, the timing control means supplying a sample completion signal to the A/D converter after all the sample and hold circuits have sampled and held the analog voltages applied to the analog signal inputs of the sample and hold circuits, so that the A/D converter starts its A/D conversion after all the sample and hold circuits have sampled and held the analog voltages applied to the analog signal inputs of the sample and hold circuits.

8. An A/D conversion circuit claimed in Claim 7 wherein the timing control means sequentially supplies the sample timing signal to the sample timing control input of the sample and hold circuits at different timings, so that the sample and hold circuits sequentially sample and hold the analog voltages applied to the analog signal inputs of the sample and hold circuits, and the timing control means supplies the sample completion signal to the A/D converter after the timing generation means has supplied the corresponding sampling timing signals to all the sample timing signals, so that the A/D converter executes its A/D conversion after all the sample and hold circuits have sampled and held the analog voltages applied to the analog signal inputs of the sample and hold circuits.

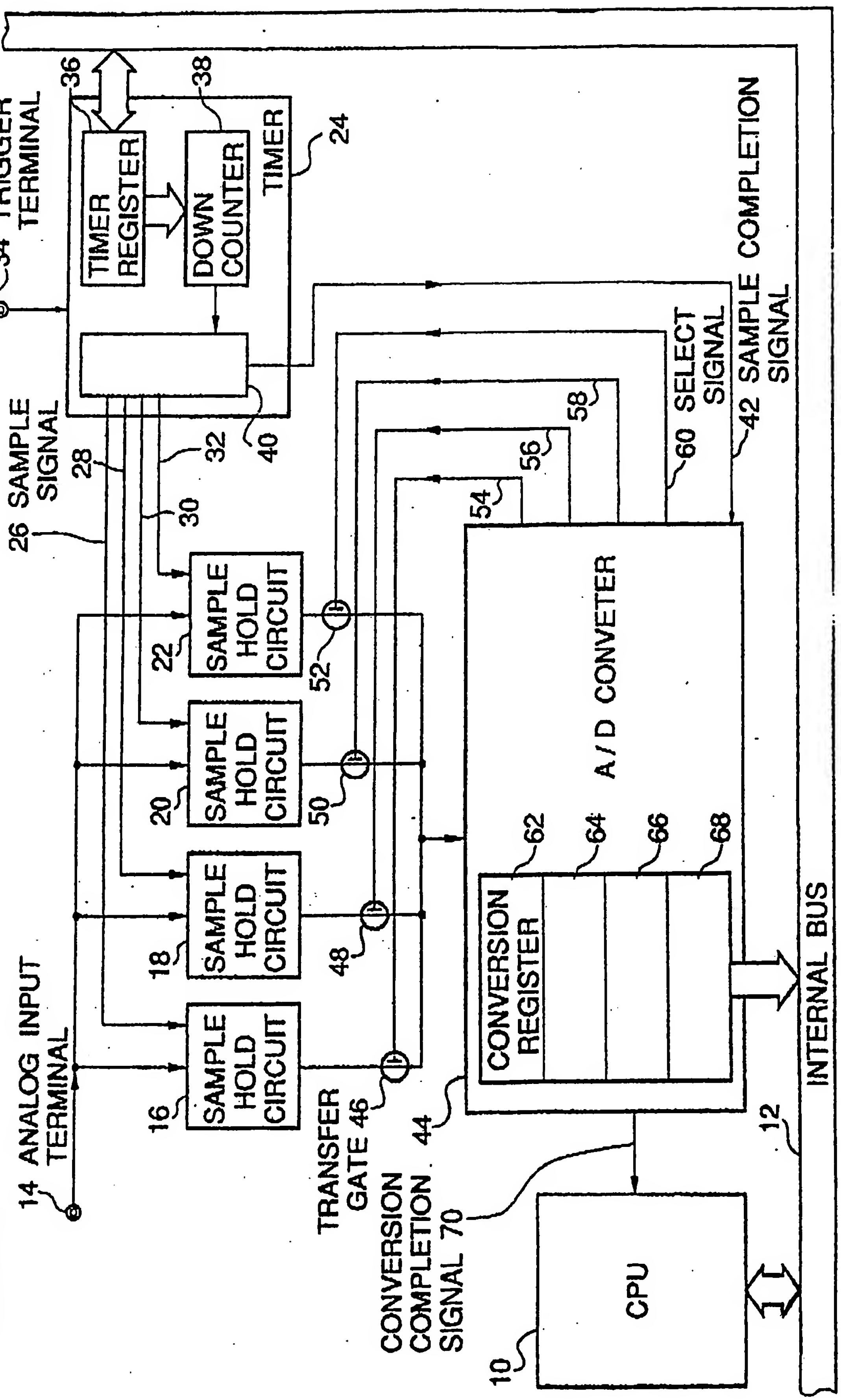

34 TRIGGER TERMINAL
36
38
TIMER REGISTER
DOWN COUNTER
TIMER
24
26 SAMPLE SIGNAL
28
30
32
40
14 ANALOG INPUT TERMINAL
16
18
20
22
SAMPLE HOLD CIRCUIT
SAMPLE HOLD CIRCUIT
SAMPLE HOLD CIRCUIT
SAMPLE HOLD CIRCUIT
TRANSFER GATE 46
48
50
52
54
56
58
60 SELECT SIGNAL
42 SAMPLE COMPLETION SIGNAL
A / D CONVETER
CONVERSION REGISTER
62
64
66
68
44
CONVERSION COMPLETION SIGNAL 70
CPU
10
12
INTERNAL BUS

FIGURE 1

# FIGURE 2

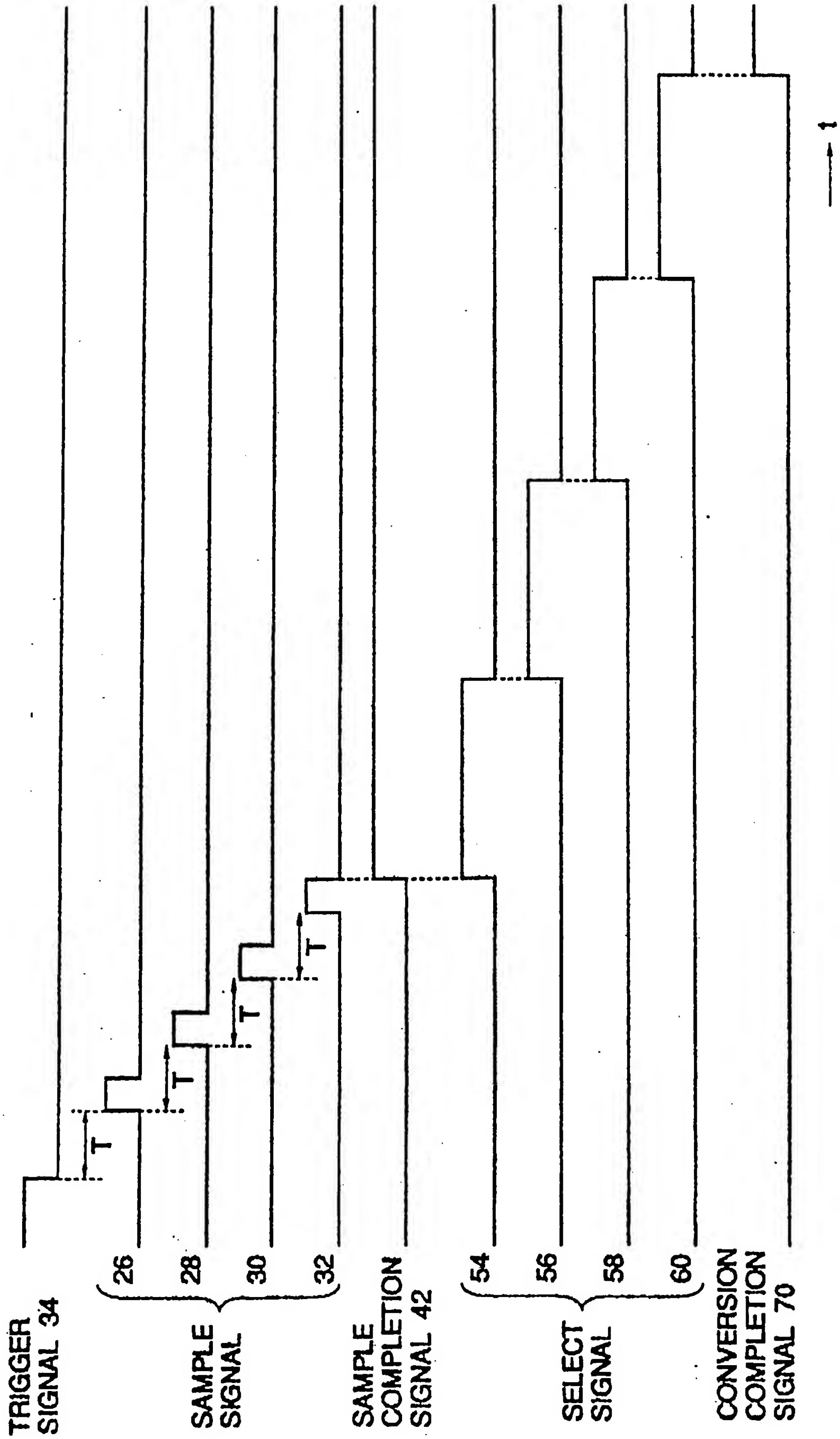
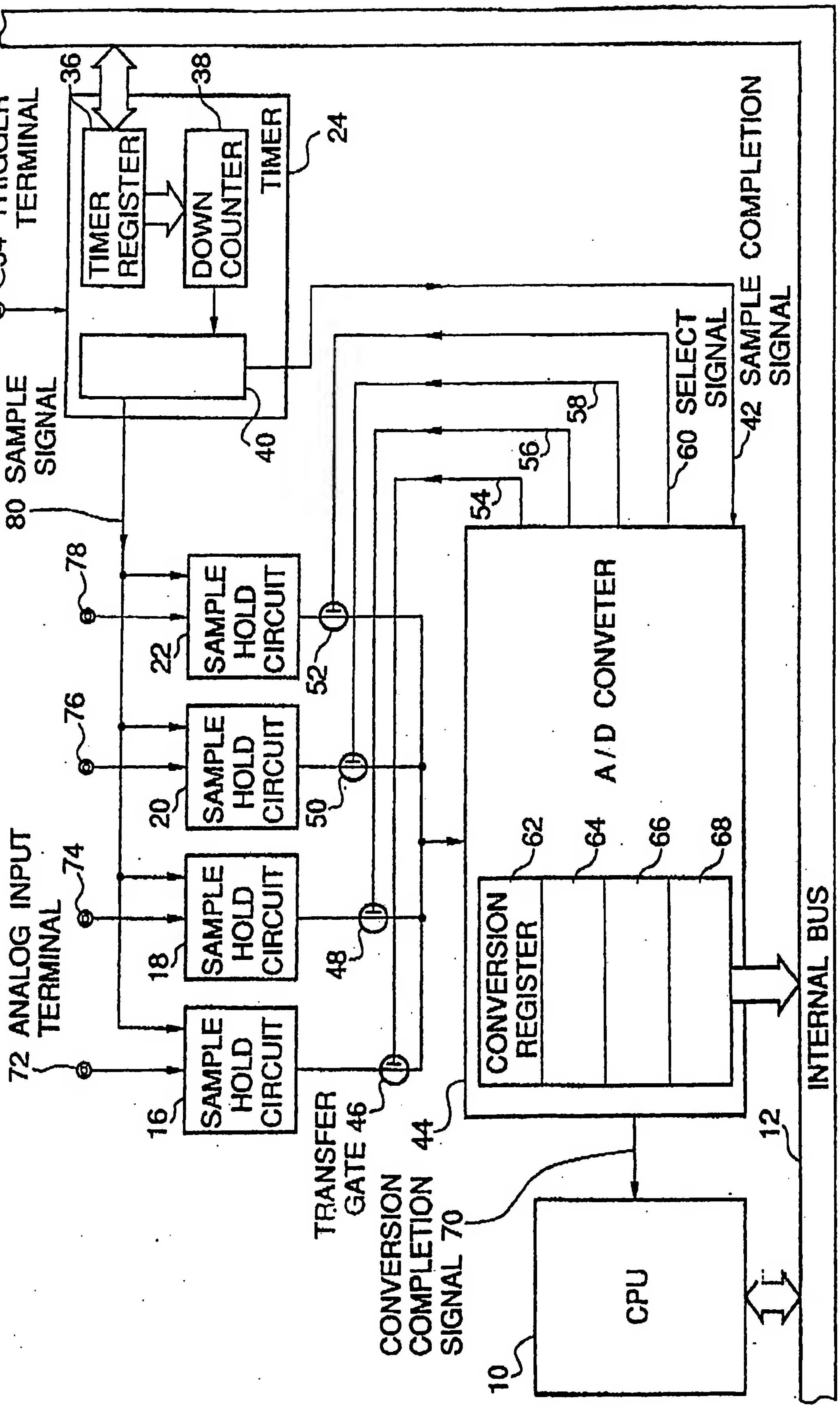

TRIGGER SIGNAL 34
SAMPLE SIGNAL
26
28
30
32
T
T
T
T
SAMPLE COMPLETION SIGNAL 42
SELECT SIGNAL
54
56
58
60
CONVERSION COMPLETION SIGNAL 70
t

FIGURE 3


34 TRIGGER TERMINAL
36
38
TIMER REGISTER
DOWN COUNTER
TIMER
24
40
80 SAMPLE SIGNAL
60 SELECT SIGNAL
42 SAMPLE COMPLETION SIGNAL
54
56
58
72 ANALOG INPUT TERMINAL
74
76
78
16
18
20
22
SAMPLE HOLD CIRCUIT
SAMPLE HOLD CIRCUIT
SAMPLE HOLD CIRCUIT
SAMPLE HOLD CIRCUIT
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CONVERSION COMPLETION SIGNAL 70
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(11) Publication number: **0 372 526 A3**

(12) **EUROPEAN PATENT APPLICATION**

(21) Application number: **89122485.9**

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(22) Date of filing: **06.12.89**

(30) Priority: **06.12.88 JP 309292/88**

(43) Date of publication of application:
**13.06.90 Bulletin 90/24**

(84) Designated Contracting States:
**DE FR GB**

(88) Date of deferred publication of the search report:
**26.08.92 Bulletin 92/35**

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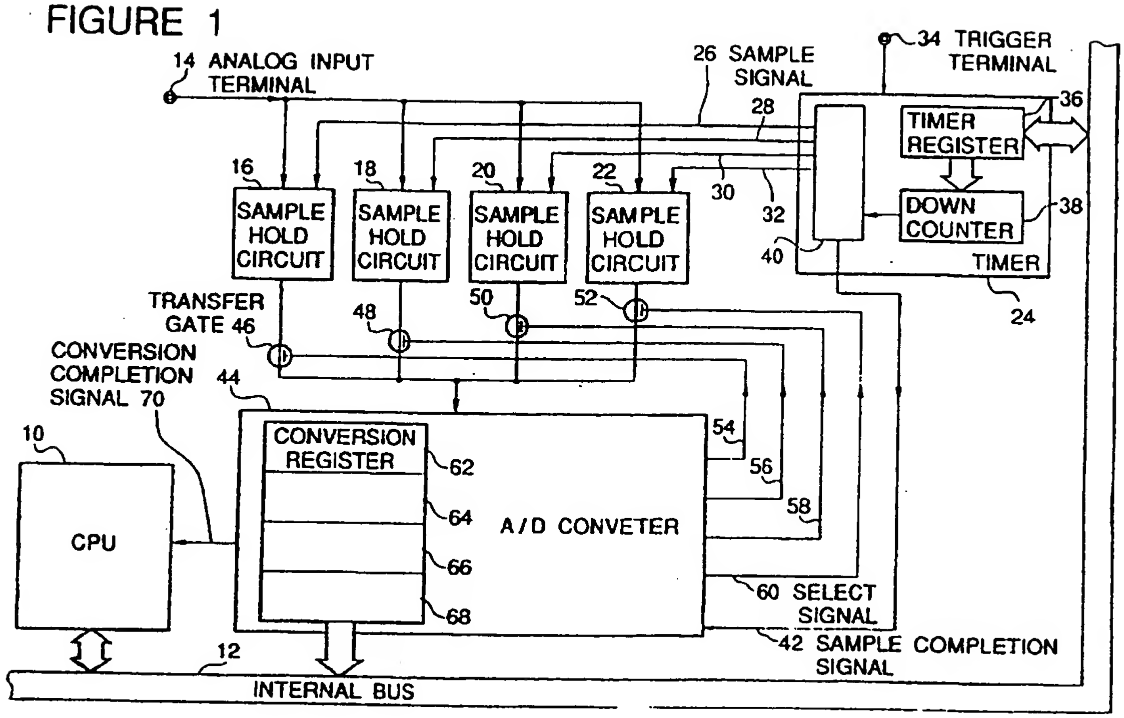
FIGURE 1


14 ANALOG INPUT TERMINAL
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42 SAMPLE COMPLETION SIGNAL
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INTERNAL BUS

European Patent Office

# EUROPEAN SEARCH REPORT

Application Number

EP 89 12 2485

## DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int. Cl.5) |
|---|---|---|---|
| A | US-A-3 493 731 (LEMONDE) 3 February 1970<br>* abstract *<br>* column 7, line 28 - column 8, line 60; figure 6 * | 1,3-4,7 | G06F3/05<br>H03M1/12 |
| A | US-A-4 364 029 (VILLA) 14 December 1982<br>* column 2, line 34 - column 3, line 4; figure 1 * | 1-3,7 | |
| A | EP-A-0 006 779 (BERNET ET AL) 9 January 1980<br>* page 3, line 8 - page 4, line 20; figure 1 * | 1-3,7 | |
| A | ELECTRONIC DESIGN<br>vol. 31, no. 20, 29 September 1983, DENVILLE NJ<br>pages 227 - 232;<br>DAVIS ET AL: 'DATA ACQUISITION MOVES INTO THE REALM OF PCS'<br>* page 228; figure 1 * | 1,3-4,7 | |
| A | ELECTRONIQUE INDUSTRIELLE<br>no. 20, May 1988, PARIS FRANCE<br>pages 28 - 33;<br>CRESCENZO ET AL: 'MICROCONTROLEUR 16 BITS'<br>* figure 1 * | 1 | TECHNICAL FIELDS SEARCHED (Int. Cl.5)<br>G06F<br>H03M |

The present search report has been drawn up for all claims

| Place of search | Date of completion of the search | Examiner |
|---|---|---|
| THE HAGUE | 25 JUNE 1992 | GUIVOL Y. |

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